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Performance Analysis of Zero Crossing DPLL with Linearized Phase Detector

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***Abstract*—This work introduces a new structure of Zero Crossing Digital Phase Locked Loop with Arc Sine block (ASZCDPLL) to linearize the phase difference detection, and enhance the loop performance. The new loop has faster acquisition, less steady state phase error, and wider locking range as compared to the conventional ZCDPLL. The locking range improvement and faster acquisition have been confirmed through simulation. The loop has been implemented and tested in real time using Texas Instruments TMS320C6416 DSP development kit.**

***Keywords*—non-uniform sampling, digital phase locked loops, zero crossing DPLL**

چکیده - ساختار جدیدی از PLL دیجیتال تقاطع صفر با بلوک سینوسی قوسی برای خطی سازی آشکار سازی اختلاف فاز و به سازی عملکرد حلقه (لوپ) پیشنهاد می گردد. این حلقه جدید از توانمندی اکتساب سریع تر خطای کمتر فاز حالت مانا و بازه قفل کردن پهن تری در مقایسه با ZCDPLL، مرسوم برخوردار است. شبیه سازی کامپیوتری موید بهتر شدن بازه قفل کردن و اکتساب سریع تر می باشد.

این حلقه به طور بیدرنگ و با به کارگیری ابزار توسعهDSP (پردازش سیگنال های دیجیتال) کمپانی Texas Instruments پیاده سازی گردیده است.

I. INTRODUCTION

Phase Lock Loops (PLLs) are widely used in variety of areas of communication applications such as carrier recovery, synchronization, and demodulation [1]. A PLL is a closed loop system in which the phase output tracks the phase of the input signal. It consists of a phase detector, filter, and voltage controlled oscillator. Digital Phase locked Loops (DPLLs) were introduced to minimize some of the problems associated with the analogue counter part such as sensitivity to DC drift and the need for periodic adjustments [2], [1]. Conventional Zero Crossing DPLL (ZCDPLL) is the most widely used due to its simplicity in modelling and implementation [3], [4].

In this paper a new structure of ZCDPLL is introduced which includes Arc-Sine block and a peak detector in addition to the main ZCDPLL main components. The purpose of including the Arc-Sine in the loop is to linearize the phase difference detection. The peak detector guarantees the input amplitude to the Arc-Sine block to remain between -1 and +1. The newly proposed Arc-Sine ZCDPLL (AS-ZCDPLL) is analyzed and simulated and its performance is compared to the conventional ZCDPLL (ZCDPLL). It has been shown that the proposed loop offers improved performance in the lock range and acquisition with reduced steady state phase error. The proposed AS-ZCDPLL can be characterized by a linear difference equation in module ($\frac{\pi}{2}$) sense. The AS-ZCDPLL loop has been implemented and tested using Texas Instruments TMS320C6416 DSP development kit. In section 2, system description of AS-ZCDPLL is given, then the first order loop stability requirement and the range of operation of the first order loop is presented in section 3. Section 4 discusses the performance of the second order ASZCDPLL. In section 5 the simulation results are presented while section 6 discusses the real time implementation of the proposed loop. Finally conclusions are given in section 7.

II. SYSTEM DESCRIPTION

The AS-ZCDPLL is composed of a sampler as a phase detector, inverse sine block, a digital loop filter and a Digital Controlled Oscillator (DCO). The input signal to the loop is taken as $x(t) = s(t)+n(t)$, where $s(t) = A\sin(\omega_0 t + \theta(t)), n(t)$ is Additive white Gaussian Noise (AWGN); $\theta(t) = \theta_0 + \Omega_0 t$ from which the signal dynamics are modelled; θ_0 is the initial phase which we will assume to be zero; Ω_0 is the frequency offset from the nominal value ω_0. The input signal is sampled at time instances t_k determined by the Digital Controlled Oscillator (DCO). The DCO period control algorithm as given by [2] is

$$T_k = T_0 - c_{k-1} = t_k - t_{k-1} \quad (1)$$

where $T_0 = (2\pi / \omega_0)$ is the nominal period, c_{k-1} is the output of the loop digital filter $D(z)$. The sample value of the incoming signal $x(t)$ at t_k is

$$x(t_k) = s(t_k) + n(t_k) \quad (2)$$

or

$$x_k = s_k + n_k \quad (3)$$

where $s_k = A\sin[\omega_0 t_k + \theta(t_k)]$. The sequence x_k is passed through the Arc-Sine block with output $y_k = \sin^{-1}(x_k)$. The output is passed through a digital filter D(z) whose output c_k is used to control the period of the DCO. The time instances t_k can be rewritten as

$$t_k = \sum_{i=1}^{k} T_i = kT_0 - \sum_{i=0}^{k-1} c_i, k = 1,2,3... \quad (4)$$

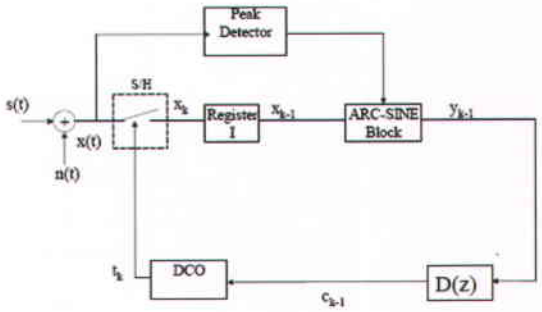

Figure 1: Block diagram of the AS-ZCDPLL

Thus

$$x_k = A\sin[\omega_0(kT_0 - \sum_{i=0}^{k-1} c_i)] + n_k \quad (5)$$

For noise free analysis $n_k = 0$, then

$$x_k = A\sin[\omega_0(kT_0 - \sum_{i=0}^{k-1} c_i) + \theta_k] \quad (6)$$

The phase error is defined to be [2]

$$\phi_k = \theta_k - \omega_0 \sum_{i=0}^{k-1} ci \quad (7)$$

Also

$$\phi_{k-1} = \theta_{k-1} - \omega_0 \sum_{i=0}^{k-2} c_i \quad (8)$$

Taking the difference of (7) and (8) results in

$$\phi_k - \phi_{k-1} = \theta_k - \theta_{k-1} - \omega_0 c_{k-1} \quad (9)$$

The Arc-Sine (sin^{-1}) block has been added to linearize the equation and avoid the nonlinear behaviour of the systems. The output of the Arc-Sine block can be expressed as $y_k = \sin^{-1}(x_k) = \phi_k$, $-1 \le x_k \le 1$, and $\frac{-\pi}{2} \le y_k \le \frac{\pi}{2}$. The z transform of the output of the digital filter is

$$C(z) = D(z)Y(z) \tag{10}$$

Where $Y(z)$ is the z transform of $y(t)$. The order of the loop is determined by the type of the digital filter. For first order, the digital filter is simply a gain block $D(z) = G_1$, where G_1 is the block gain. However, for second order loop, $D(z) = G_1 + \frac{G_2}{1-z^{-1}}$ as will be shown in what follows.

III. FIRST ORDER AS-ZCDPLL

In this paper, the behaviour of the first order AS-ZCDPLL for an input with frequency offset in the absence of noise is analyzed and simulated. If the input to AS-ZCDPLL is a frequency step with $\Omega_0 = (\omega - \omega_0)$ is applied, then $\theta_k = (\omega - \omega_0)t_k$. Using (4), then

$$\phi_k - \phi_{k-1} = (\omega - \omega_0)T_0 - (\omega - \omega_0)c_{k-1} \tag{11}$$

(9) can also rewritten as

$$\phi_k = \phi_{k-1} - k_1\phi_{k-1} + \Lambda_0 \tag{12}$$

where

$\Lambda_0 = (\omega - \omega_0)T_0 = 2\pi\frac{(\omega - \omega_0)}{\omega_0}$, $K_1 = \omega G_1$. The steady state phase error ϕ_{ss} must satisfy

$$\phi_{ss} = (1 - K_1)\phi_{ss} + \Lambda_0 \tag{13}$$

Since $\phi_k = \phi_{k-1} = \phi_{ss}$ in the steady state. Accordingly ϕ_{ss} will be $\phi_{ss} = \frac{\Lambda_0}{k_1}$.

In order for the loop to achieve locking, first ϕ_{ss} must lie in the interval $(-\frac{\pi}{2}, \frac{\pi}{2})$ and this comes from the properties of the inserted arc sine block, or

$$\left|\frac{\Lambda_0}{K_1}\right| \le \frac{\pi}{2} \tag{14}$$

This will lead to that $K_1 > 4\frac{\omega - \omega_0}{\omega_0}$.

Let $\psi_k = \phi_k - \phi_{ss}$, the equation (12) can be rewritten as

$$\Psi_k = (1 - K_1)\psi_{k-1} \tag{15}$$

Taking the z-transform of both sides of equation (15) and solving for $\Psi(z)$, then

$$\Psi(z) = \frac{\psi(0)z}{z - (1 - K_1)} \tag{16}$$

the loop will be locked if the roots of the denominator lies inside the unit circle and this will lead to the inequality

$$|1 - K_1| < 1, K_1 < 2 \tag{17}$$

The steady state phase error ϕ_{ss} of the first order conventional ZCDPLL (ZCDPLL) for an input with frequency offset is give by [7]:

$$\phi_{ss} = \sin^{-1}(\frac{\Lambda_0}{K_1}), for \frac{\Lambda_0}{K_1} < 1 \tag{18}$$

Since $\left|\frac{\Lambda_0}{K_1}\right| < \left|\sin^{-1}(\frac{\Lambda_0}{K_1})\right|$ for $\left|\frac{\Lambda_0}{K_1}\right| < 1$, it is clear that steady state phase error of AS-ZCDPLL is always less than that of ZCDPLL for the same values of Λ_0, and K_1. Another advantage of AS-ZCDPLL is that the gain $K_1 = \omega G_1$ is independent of the signal power, while ZCDPLL gain $K_1 = AwG_1$ is power dependent. For optimum value of filter gain, the loop could go into instability if the signal power increases. The ZCDPLL requires an Automatic Gain Control (AGC) circuit to overcome this problem. It is also interesting to show the performance of AS-ZCDPLL when the frequency is varied with the same value of G_1 (filter gain). Define

$K = G_1\omega_0 = K_1\frac{\omega_0}{\omega}$. Since $\Lambda_0 = 2\pi(\frac{\omega}{\omega_0} - 1)$, then the lock range can be expressed as

$$4\left|1 - \frac{\omega}{\omega_0}\right| < K_1 < 2 \tag{19}$$

Figure (2) shows that the lock range of the first order ASZCDPLL for different values of K and $\frac{\omega_0}{\omega}$ (area enclosed between the lines (3),(4), and (5)), together with ZCDPLL obtained from [7] (Area enclosed between curves (1) and 2)). It is clearly shown that AS-ZCDPLL has wider lock range.

IV. SECOND ORDER AS-ZCDPLL

As mentioned earlier, for second order ZCDPLL the digital filter $D(z) = G_1 + \frac{G_2}{1-z^{-1}}$, then (10) becomes

$$C(z) = (G_1 + \frac{G_2}{1-z^{-1}})Y(z)$$

$$C(z)(1 - z^{-1}) = (G_1(1 - z^{-1}) + G_2)Y(z) \tag{20}$$

To express in time domain

$$c_k = c_{k-1} + (G_1 + G_2)y_k - G_1 y_{k-1} \quad (21)$$

Since $y_k = \phi_k$, and by replacing k by $(k\text{-}1)$ into equation (21), then

$$c_{k-1} - c_{k-2} = (G_1 + G_2)\phi_{k-1} - G_1\phi_{k-2} \quad (22)$$

Replacing k by k-1 in equation (11) results in

$$\phi_{k-1} - \phi_{k-2} = (\omega - \omega_0)T_0 - (\omega - \omega_0)c_{k-2} \quad (23)$$

Taking the difference of (23) and (11) leads to

$$\phi_k - 2\phi_{k-1} + \phi_{k-2} = \omega(c_{k-2} - c_{k-1}) \quad (24)$$

Replacing $c_{k-2} - c_{k-1}$ of equation (22) into equation (24) results in

$$\phi_k - 2\phi_{k-1} + \phi_{k-2} = -\omega((G_1 + G_2)\phi_{k-1} - G_1\phi_{k-2}) \quad (25)$$

Let $r = 1 + \frac{G_2}{G_1}$, and $k_1 = \omega G_1$ then

$$\phi_k = (2 - K_1 r)\phi_{k-1} + (K_1 - 1)\phi_{k-2} \quad (26)$$

Define the system state vector
$x_k^1 = y_{k-2}, x_k^2 = y_{k-1}, X = (x^1, x^2)^T$, then

$$\begin{pmatrix} x_{k+1}^1 \\ x_{k+1}^2 \end{pmatrix} = \begin{pmatrix} x_k^2 \\ (K_1 - 1)x_k^1 + (2 - K_1 r) \end{pmatrix} = \begin{pmatrix} g_1(x) \\ g_2(x) \end{pmatrix} = G(x_k) \quad (27)$$

The Jacobian $G'(X) = \partial_{g_i} / \partial_{x^j}$ is given by

$$G'(X) = \begin{pmatrix} 0 & 1 \\ K_1 - 1 & 2 - K_1 r \end{pmatrix} \quad (28)$$

In order to have Eigen values of G'(x) less than 1, or $|\lambda_i| < 1, i = 1,2$, where $|\lambda_i|$ satisfies the characteristic equation $F(\lambda) = |\lambda I - G'(X^*)| = 0$ [5]

$$F(\lambda) = \lambda^2 - (2 - K_1 r)\lambda - (K_1 - 1) = 0 \quad (29)$$

Using Jury stability test [5], the roots of the polynomial $F(\lambda)$ defined in (29) will have roots within a unit circle, or the eigenvalues are less than 1, if $(-1)^2 F(-1)$ greater than 0. This will lead that K_1 should be less than $\frac{4}{r+1}$ to ensure stable loop behaviour. Also from the Jury stability test applied on $F(\lambda)$, $|K_1 - 1|$ should be less than 1 or $K_1 < 2$, so r should be greater than 1, which of course is the same as [8] but without linearizing the equations. Figure (3) shows the second order loop stability region. For optimum values in terms of acquisition time, $K_1 = 1$, and $r = 2$ [8].

Assume $K_{10} = \omega_0 G_1$, which is independent of the frequency as the nominal frequency ω_0 is assumed to be constant, then $K_1 = K_{10}\frac{\omega}{\omega_0}$, therefore the second order frequency acquisition range becomes:

$$\frac{r+1}{4}K_{10} < \frac{\omega_0}{\omega} < \infty \quad (30)$$

The borders on $K10$ for stability as a function of $\frac{\omega_0}{\omega}$ in Figure (4) under the condition $r = 2$. For second order loop, there is no limit to the amount of ω can decrease for a given value of $K10$, but there is a limit to the increase in the frequency above the nominal value.

V. SIMULATION RESULTS

The operation behaviour of the AS-ZCDPLL has been verified by simulation. Consider a modulation free input signal $y(t) = \sin(\omega_1 t)$, where ω_1 is the input frequency, the center frequency of the DCO is assumed to be $\omega_0 = 1$ rad/sec. After discarding the first 100 points, the next 100000 points are collected and recorded to produce bifurcation. The bifurcation plot of the first order AS-ZCDPLL is provided in figure (5) for different values of the filter gain.

To verify that AS-ZCDPLL has better acquisition time compared to ZCDPLL, the loop is subjected to a frequency step with random initial phase. The acquisition time is estimated and recorded when the loop starts converging to the desired frequency. This operation is repeated 100 times with random initial phase and the acquisition time is recorded for that frequency step. It can be seen from figure (6) that ASZCDPLL has faster accusation time compared to ZCDPLL for all frequency offsets. K_1 has been kept constant through the simulation and set to be equal to 1 which is optimum value for the loop. The AS-ZCDPLL has been tested with Frequency Shift Keying (FSK) input signal with random transmitted data and it can be seen from figure (7) that the AS-ZCDPLL operation is better than its equivalent ZCDPLL.

The second order AS-ZCDPLL bifurcation plot is shown in figure (8). The loop parameter r is assumed to be 2, while $K1$is varied. The figure shows that the second order AS-ZCDPLL has wider locking range compared to the conventional second order ZCDPLL. Second order AS-ZCDPLL has faster acquisition time as shown in Figure (9).

VI. SYSTEM IMPLEMENTATION

To test the loop under real time conditions, the first order loop has been selected for this purpose. The loop has been implemented in the software code targeted at a Texas Instruments TMS320C6416 DSP. The key issue in the realization of ASZCDPLL is the implementation of variable sample rate signal processing and inverse sign block. In the realization based of DSP, variable sampling rate can be

efficiently implemented using the DSP chip timer. At the beginning of the software program, the DSP timer (e.g Timer1) is set to be equal to maximum value of the sampling period. While the timer counts towards zero, an input (error) sample is read from the Analogue to Digital converter (ADC). On the basis of zthe error sample, the controller output and the actual value of the sampling period T are computed. Then the computed value of

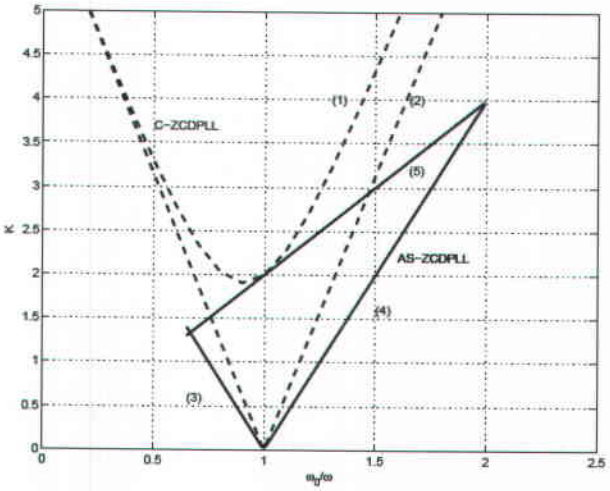

Figure 2: Lock Range of first order AS-ZCDPLL compared to ZCDPLL

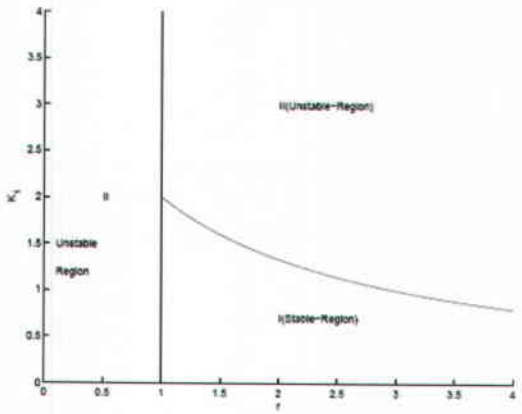

Figure 3: Loop behaviour as a function of $K1$ and r for second-order ZCDPLL

the sampling period is used to set the timer period. The DSP processor will enter an idle state till the timer expired, then the processed will be interrupted and the Interrupt Service Routine (ISR) will be called and the program loop repeats. Real-Time Data Exchange (RTDX) is used to provide real time, continuous visibility into the way AS-ZCDPLL software application operates in TMS320C6416. RTDX allows transfer the random bits generated in the DSP to a host PC for testing. On the host platform, an RTDX host library operates in conjunction with Code Composer Studio. In RTDX an output channel should be configured within AS-ZCDPLL software. Data is written to the output channel. This data is immediately recorded into a C6416 DSP buffer defined in the RTDX C6416 library. System block diagram of the implemented system is shown in figure (10). The data from this buffer is then sent to the host PC through the JTAG interface. The RTDX host library receives this data from the JTAG interface and records it into either a memory buffer for testing purposes. To approximate $\sin^{-1}(.)$, the following is proposed in this

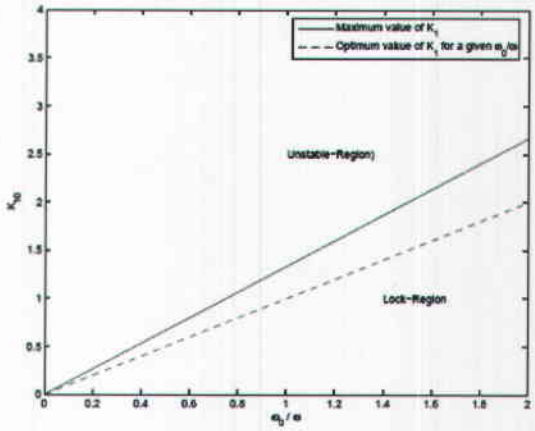

Figure 4: Frequency acquisition region as a function of K_{10} and $\frac{\omega_0}{\omega}$ for second-order ZCDPLL

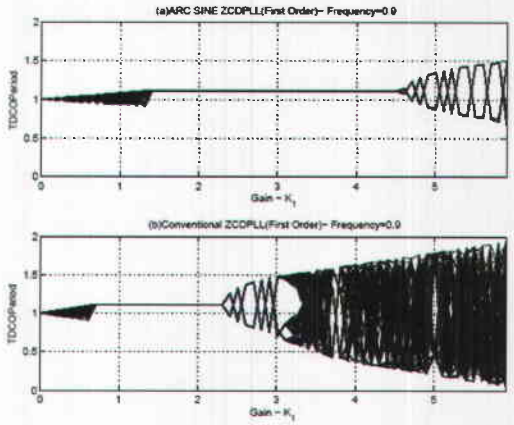

Figure 5: Bifurcation of First order AS-ZCDPLL compared to ZCDPLL

work. Recall the following integral formula [9]:

$$\sin^{-1}(x) = \int_0^x (1-t^2)^{-\frac{1}{2}} dt \qquad (31)$$

Also recall

$$(1+x)^\alpha = 1 + \binom{\alpha}{1}x + \binom{\alpha}{2}x^2 + \binom{\alpha}{3}x^3 + \ldots \qquad (32)$$

The above equation holds for any real number α, where the binomial number is [9]:

$$\binom{\alpha}{k} = \frac{\alpha.(\alpha-1)....(\alpha-k+1)}{k!} \qquad (33)$$

Now let $\alpha = -\frac{1}{2}$, then

$$(1-t^2)^{-\frac{1}{2}} = 1+\left(\frac{-\frac{1}{2}}{1}\right)\left(-t^2\right)+\left(\frac{-\frac{1}{2}}{2}\right)\left(-t^2\right)^2+... \quad (34)$$

So equation (20) will be as

$$\sin^{-1}(x) = \int_0^x 1dt + \int_0^x \left(\frac{-\frac{1}{2}}{1}\right)\left(-t^2\right)dt + \int_0^x \left(\frac{-\frac{1}{2}}{2}\right)\left(-t^2\right)^2 dt + ... \quad (35)$$

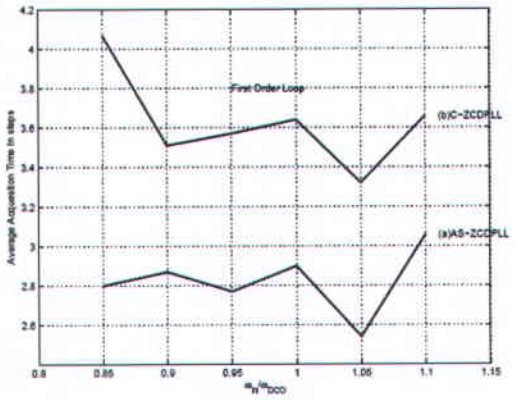

Figure 6: Acquisition Time of first order AS-ZCDPLL compared to ZCDPLL

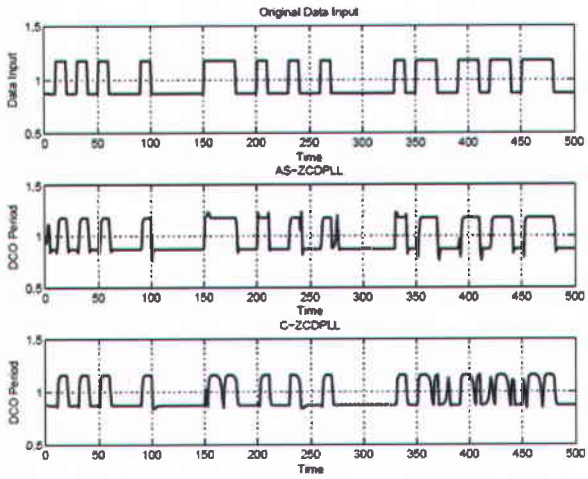

Figure 7: FSK performance of first order AS-ZCDPLL compared to ZCDPLL

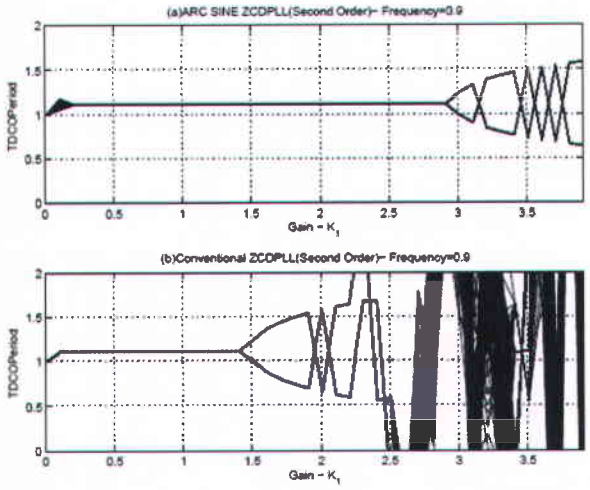

Figure 8: Bifurcation of second order AS-ZCDPLL compared to ZCDPLL

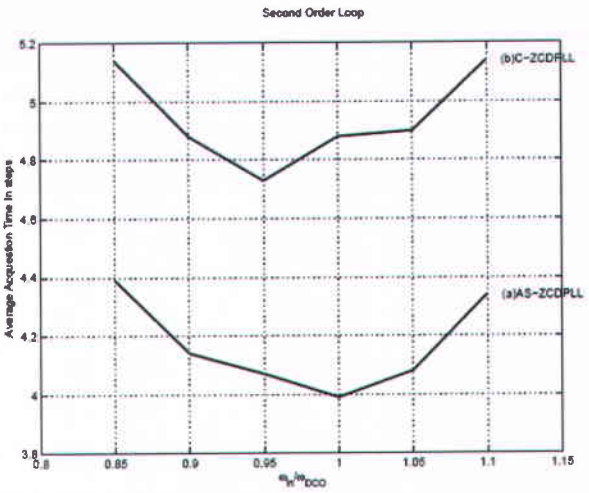

Figure 9: Acquisition Time of second order AS-ZCDPLL compared to ZCDPLL

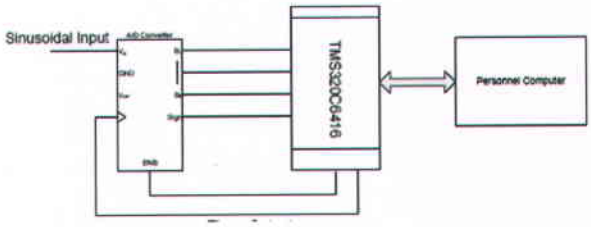

Figure 10: TMS320C6416 Based AS-ZCDPLL

Using equation (22), equation (24) will be after taking only three terms:

$$\sin^{-1}(x) \approx x + \frac{1}{6}x^3 + \frac{3}{40}x^{-5} \quad (36)$$

In the DSP implementation only two terms has been taken. Figure (11) shows MATLAB plot of actual sin^{-1} and two terms approximation of the arc sine using the above approach.

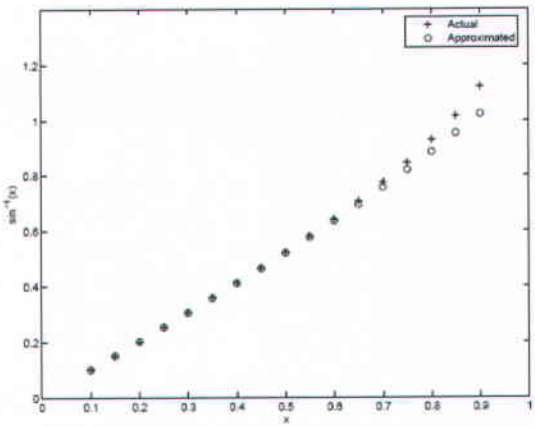

Figure 11: sin^{-1} Approximation compared with Actual one

VII. CONCLUSIONS

It has been shown that the proposed AS-ZCDPLL loops have many attractive features compared to the conventional ZCDPLL. These include faster

acquisition, wider lock range, insensitivity to input signal power variation and reduced steady state phase error. The proposed loops have shown a clear performance improvement over the conventional one as shown in figures (4, 5, 7, and 8). Also the AS-ZCDPLL can have smaller values of gain compared to ZCDPLL and thus it has more immunity to noise. The first order AS-ZCDPLL has been implemented and tested in real time using Texas Instruments TMS320C6416 DSP development kit.

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